REMARKS

In response to the Notice of Drawing Inconsistency With Specification, applicant is herewith submitting replacement pages 4 and 6-9 of the Specification. On these replacement pages, the designations of drawing figures are being corrected to correspond with the original drawing figures. The addition of "new matter" has been scrupulously avoided.

The Notice received by applicants from the USPTO also states that Figure 15f is listed in the Brief Description of the Drawings in the Specification, but not contained in the Drawings. Applicants respectfully submit that this objection is erroneous since original drawing sheet 16/16 includes Figure 15f below Figure 15e. A duplicate copy of this drawing sheet is enclosed.

Since all of the identified deficiencies have been addressed, applicants request that this application be processed for grant.

If there are any questions regarding this response, please call applicants' attorney at the below indicated telephone number.

Respectfully submitted,

Jeff Rothenberg
Reg. No. 26,429
Attorney for Applicants

Dated: June 29, 2007

Heslin Rothenberg Farley & Mesiti P.C.
5 Columbia Circle
Albany, New York 12203
Tel: 518-452-5600
Fax: 518-452-5579
E-mail: jr@hrfmlaw.com

the trough. A further possibility for separation is done by providing the semiconductor substrate with slots or incisions that extend into the trough (trench insulation).

In the following, several illustrative embodiments of the process for producing transistors or logic gates are described by detailed reference to the accompanying drawings, wherein:

Figures 1a to 1c depict the step in production of an n-doped trough in the semiconductor substrate using high energy ion implantation, whereby the mask defining the window for ion implantation is delimited by an edge running perpendicular or tilted inward or outward;

Figures 2a to ~~2d~~ 2e depict the further process steps for producing an NPN-transistor starting with the semiconductor structure depicted in Figures 1a to 1c;

Figures 3a to ~~3d~~ 3e depict the further process steps for producing a PNP-transistor starting with the semiconductor structure depicted in Figures 1a to 1c;

Figures 4a to ~~4e~~ 4f depict the further process steps for producing an alternative embodiment of an NPN-transistor that is characterized by a high gain and based on the semiconductor structure depicted in Figures 1a to 1c;

Figures 5a to ~~5d~~ 5edepict the individual process steps for producing an I^2L (Integrated Injection Logic) element, starting with the semiconductor structure depicted in Figures 1 to 1c;

Figures 6a to ~~6e~~ 6f depict the individual process steps for producing a field effect transistor starting with the semiconductor structure depicted in Figures 1a to 1c, and

Figures 7a to 7f depict the individual process steps for producing a logic gate with implanted insulation;

Figures 8a to 8e depict the individual process steps for producing a logic gate with low-frequency modulate trough and implanted insulation;

Figures 9 a to 9e depict the individual process steps for producing a logic gate with low-frequency modulated trough and oxide insulation;

Figures 10a to 10f depict the individual process steps for producing a logic gate with trench insulation, and

With high-energy implantation there is a peculiar effect in the area of the edge 4 of the mask window 3. Since the ions are scattered at the vertical edge or are slowed down at different intensities at the slanted edges, a fringe area 7 forms extending upwards in the trough 5, said area extending as far as the surface of the semiconductor substrate 1 and encloses the remaining p-doped area 6 at the surface of the semiconductor substrate.

To produce an integrated circuit and by using an appropriate mask, a number of n-dopes troughs, whose fringe areas extend to the semiconductor substrate surface, can be inserted using ion implantation.

Alternatively, however, ion implantation can also be done using an energy that is sufficient to cause a p-doped inner area to remain at the surface of the semiconductor substrate. For example, at an implantation energy of 2 MeV and a does of 2×10^{13} atoms/cm^2, the back-scattered phosphorus ions reach the surface of the wafer in sufficient number and no weakly p-doped area remains but an n-doped semiconductor with a concentration of $N_p > 10^{15}/cm^{-3}$ does. This is prevented in that either a wafer with an overall higher p-concentration is used as the starting material or additional doping is inserted into the wafer surface for the purpose of compensation. This can be done by implantation or diffusion. For example, compensation can be produced with an implantation energy of 200 KeV and a dose of 3×10^{11} atoms/cm^2 to a depth of 8 µ. However, these are merely reference values that can be changed multiply. The re-doping can be done over the entire surface or only within the trough using a mask.

Starting with the semiconductor structure described with reference to Figures 1a to 1c various transistor types can be produced.

Figures 2a to ~~2d~~2e illustrate the steps for producing an NPN-transistor. In the p-doped inner area 6 of the semiconductor structure (Figure 2a) enclosed by the n-doped trough of Figures 1a to 1c, a central rectangular, round or other shaped p-doped area 8 is inserted using ion implantation and using conventional doping ($N_A = 10^{18} cm^{-3}$) which is heavier than that of the semiconductor substrate (Figure 2b). Then, using ion implantation, a shallow peripheral n^+-junction area 9 having the convention doping concentration ($N_p \sim 10^{22} cm^{-3}$) in the fringe area 7 of the trough 5 and a shallow n^+-doped area 10 ($Np = 10^{22} cm^{-3}$) is inserted in the p-doped area 8 enclosed by the inner area 6 (Figure 2c). In a further implantation step a shallow p^+-doped junction area 11 ($Np = 10^{22} cm^{-3}$) is inserted into the p-doped area 8 (Figure 2d). Finally, the insulation area (not shown) can be constructed and the bonding of the transistor connectors to the n^+ or

the p^+ junction areas can be done using the conventional processes (*vide supra:* G.R. Wilson). In this illustrative embodiment the n-doped through 5 forms the collector C, the p-doped inner area 6 together with the p-doped area 8, the base B, and the n^+-doped area 10 forms the emitter of the NPN-transistor (Figure 2e).

Production of a PNP-transistor likewise starts with the semiconductor structure depicted in Figures 1a to 1c. Using ion implantation, a central n-doped area 12 ($Np=10^{18}cm^{-3}$) is inserted (Figure 3b) into the p-doped inner area 6 (Figure 3a). Then, using ion implantation, a peripheral shallow n^+-junction area 13 ($Np=10^{22}cm^{-3}$) is inserted into the fringe area 7 of the trough 5 and a shallow, lateral n^+-junction area 14 ($Np=10^{22}\ cm^{-3}$) is inserted into the n-area 12 (Figure 3c). Then, in a further process step, a peripheral shallow p^+-junction area ($Np=10^{22}cm^{-3}$) is inserted into the inner area 6 and a lateral shallow p^+-area 16 ($Np=10^{22}cm^{-3}$) is inserted into a central n-area 12 using ion implantation. The p-inner area 6 now forms the collector C, the central n-area 12 the base B and the p^+-area 16 the emitter E of the PNP-transistor, whereby the highly-doped junction areas are provided for producing an ohmic connection to the transistor terminals (Figures 3d and 3e). The bonding of the transistor terminals can be done using conventional processes. In order to increase the turnover/breakdown voltage between emitter and collector, in practical applications base and trough can be electrically connected to one another.

Figures 4a to 4e4f depict the process steps for producing a further embodiment of an NPN-transistor that is characterized by a high gain (super-beta-transistor). Starting with the semiconductor structure (Figure 4a) of Figures 1a to 1c, an n-doped area 17 ($Np=10^{18}cm^{-3}$)-is produced in the inter area 6 by means of ion implantation (Figure 4b). Then, using ion implantation, a peripheral shallow n^+-junction area 18 ($Np=10^{22}cm^{-3}$) in the fringe area 7 of the trough 5 and a shallow n^+-junction area 19 ($Np=10^{22}cm^{-3}$) in the n-area 17 are produced by means of ion implantation (Figure 4c). Thereafter a shallow p^+-junction area 20 ($Np=10^{22}cm^{-3}$) is produced in the inner area 6 of the base B, and the n-area 17 the emitter E of the super-beta-NPN-transistor. At the junction areas 18, 19, and 20 bonding of the transistor terminals is again done. In the above embodiment of the invention, the stack consisting of the n-doped area 17 and the n^+-doped area 19 are not unconditionally required; in principal, the n^+-doped area 19 is sufficient. The stack, however, reduces the risk of metallic shorting, wherein by the efficacy is improved. The n^+-doped area 19 does not even have to lie within the n-doped area 17. Areas 17 and 19 can also overlay or only partially overlap each other.

Figure ~~4e~~ 4f depicts a partial view of the embodiment as described in Figures 4a to ~~4d~~4e, in which the n^+-doped area 19 and the n-doped area 17 overlay each other without area 19 being enclosed by area 17.

Figures 5a to ~~5d~~5e depict the process steps for producing an I^2L element starting with Figures 1a to 1c. Initially n-doped areas, for example four n-doped areas, 21, 22, 23, 24 ($Np=10^{18}cm^{-3}$) are inserted into the inner area 6 by means of ion implantation. Area 21 extends from the fringe area 7 of the trough 5 into the fringe region of the inner area 6 (Figure 5b). In the next process step, a peripheral shallow n^+-junction area 25 ($Np\sim10^{22}cm^{-3}$) in the fringe area 7 of the trough 5 and in the n-doped areas 22, 23, 34 further shallow n^+-junction areas 26, 27, 28 ($Np=10^{18}cm^{-3}$) are produced using ion implantation. In the n-area 21 that connects the fringe area 7 of the trough 5 with the inner area 6 a shallow p^+-doped area 29 ($Np=10^{22}cm^{-3}$) is produced. A further p^+-junction area 30 ($Np=10^{22}cm^{-3}$) is inserted into the inner area laterally adjacent to the n^+-junction areas 26, 27, 28. The inner area 6 then forms the base of a multi-collector transistor, while the n-areas 22, 23, 24 form the individual collectors C1, C2, C3 of the inversely operated transistor. The injector terminal INJ is created at the p+ area 29 and the terminal of the base B at the junction area 30 and the collectors C1, C2, C3 at the junction areas 26, 27, 28 using conventional bonding processes (Figure 5e).

The feed of the current into the I^2L element via an injection PNP is only a preferred version. Even a high-ohm resistance or a current source / power supply are conceivable.

Figures 6a to ~~6e~~6f depict the process steps for producing a field effect transistor which is characterized by high turnover/breakdown voltage and slope. Fabrication is based on Figures 1a to 1c (Figure 6a). Using ion implantation, a rectangular n-doped area 31 is inserted into the p-doped inner area 6 of the trough 5; said rectangular n-doped area extends over the entire width, but not ober the entire length of the inner area 6, such that the inner area is separated into two regions (Figure 6b). Then, using ion implantation, a peripheral shallow n+ junction area 32 ($Np=10^{22}cm^{-3}$) is inserted into the fringe area 7 of the trough 5 and a shallow n+ junction area 33 ($Np=10^{22}cm^{-3}$) is inserted into the n-area 31. Said areas form the gate of the transistor (Figure 6c). Then, in each of the two regions of the inner area 6 one p^+-doped area 34 ($Np=10^{22}cm^{-3}$) is produced (Figure 6d). The p^+-doped implants 34 represent the junction areas for metal bonding of drain and source of the transistor (Figure ~~6d~~6e). Figure ~~6e~~6f depicts the field effect transistor viewed from above.

The method for producing the various transistor types is advantageous inasmuch as the costly epitaxy and insulation steps are eliminated. All transistor types can be produced starting with the

same semiconductor structure using the described process steps simultaneously in a common production process. The individual process steps for producing the n-doped or p-doped areas in the semiconductor structure can also be done in a sequence other than that described in the above illustrative embodiments. Generally, arsenic or phosphorous ions with an energy of 5 to 5o keV are used for n+ implant ions. The energies for the n-implant ions are correspondingly higher at 30 to 100 keV. In p- and p+ implant ions generally boron ions are used with comparable energies as in the n-and n+ implant ions. The indicated concentrations and energies are values used in practice and can be increased or decreased. Other methods for introducing the doping are also possible. Interruptions of the doped areas are likewise possible. n and n^+ or p and p+ as stacks with or without overlap are not absolutely necessary; n+ or p^+ are sufficient. If, however, an n and a p implant ion are below, this arrangement reduces the risk of metal shorting by the n+ or p+ layers and consequently improves efficacies and can change the electrical data of the components. With the base terminal and drain/source n or p can be underlying. Therein the masking can be done using the photolithographic processes in the practice.

In order to make possible a particular low-impedance bulk resistor it is advantageous if the junction area in the fringe area of the n-doped trough is not designed as a shallow area but as an area that extends deeper into the semiconductor substrate. Thus, the junction area can, for example, extend to a depth at which the n-doped trough lies. However, to achieve this an additional process step is required.

The geometric arrangement of collector, emitter, and base in the trough is depicted in the illustrations for exemplar purposes only. Both size and length can be changed. Structures described as rectangles can have also other shapes; for example, round shapes.

Along with the components described above, further logic gate types can be produced in a common production process starting with the semiconductor structure described with reference to Figures 1a to 1c. Figures 7 to 10 depict the individual steps of various methods for producing logic gates, which are based on said semiconductor structure,